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UNIVERSITY OF MSILA
COMPUTER SCIENCE DEPARTMENT

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1h:30

Stucture Machine 2
EXAM nswers

Student Information

First Name: .....

Last Name: .....

Group: .....

Final Mark

_____

Exam Instructions

- Read all questions carefully.
- Answer all questions in the space provided.
- A multiple-choice answer is correct only if you select **all** and **only** the correct choices.
- No mobile phones or smart watches are allowed.
- Manage your time wisely.

1. A combinational circuit the next state is computed as :
   - ☐ a function of previous state
   - ■ **a function of the inputs only**
   - ☐ a function of the inputs and outputs.
   - ☐ a function of the inputs and previous state.
   - ☐ a function of the clock.

2. A Full-adder can perform addition on:
   ☐ 1 bit ☐ 1 bit + carry-in ☐ 2 bits ■ **2 bits + carry-in**

3. A half-adder can perform addition on:
   ☐ 1 bit ☐ 1 bit + carry-in ■ **2 bits** ☐ 2 bits + carry-in

4. The sum expression (S) in a Full-adder is:
   ☐ $A + B$ ☐ AB ■ $A \oplus B \oplus C_{in}$ ☐ $AB \oplus C_{in}$ ☐ $A \oplus B$ ☐ $(A + B) \oplus C_{in}$

5. We can implement a 3-variable function with :

   ☐ 4x1 Mux only ■ **4x1 Mux and logic gates.** ■ **8x1 Mux only.** ■ **Two 4x1 Mux with enable line.** ☐ Two 4x1 Mux without enable line.

6. Which of the following is not a combinational circuit?:

   ☐ Adder ☐ Subtractor ■ **Register** ☐ Decoder ☐ Demultiplexer ■ **JK-Flipflop** ■ **Counter** ☐ Comparator ☐ Multiplier

7. A demultiplexer with fixed high input is a :

   ☐ Multiplexer ■ **Decoder** ☐ Subplexer ☐ Encoder ☐ One bit Multiplier

8. The expression of borrow output in a half-subtractor is $\bar{A}B$:

9. A 3 bit multiplier has **6** outputs.

10. A 3 bit magnitude comparator has **3** outputs

11. An active LOW SR-LATCH S=0 and R=1 is

    ■ **Set** ☐ Rest ☐ Memory ☐ Latch ☐ Forbidden ☐ Undefined

12. An active LOW SR-LATCH S=0 and R=0 is

    ☐ Set ☐ Rest ☐ Memory ☐ Latch ■ **Forbidden** ■ **Undefined**

13. An active HIGH SR-LATCH S=0 and R=0 is

    ☐ Set ☐ Rest ■ **Memory** ■ **Latch** ☐ Forbidden ☐ Undefined

14. A D-Latch is made from :

    ☐ SR-Latch ☐ Master/Slave SR-Latch ■ **Gated SR-Latch** ☐ D-flipflop

15. What is the difference between a latch and a flipflop

    ☐ no difference ☐ latches are edge triggered ■ **flipflops are edge triggered** ■ **latches are level triggered.** ☐ flipflops are level triggered.

16. An SR-flipflop is made from

    ☐ One SR-latch. ☐ One Gated SR-latches. ☐ One D-Latch. ☐ Tow SR-latches. ■ **Two Gated SR-Latches.** ☐ Two D-latches.

17. A D-FlipFlop where $\bar{Q}$ is connected to D acts like :

    ☐ T-Latch ■ **T-FF** ☐ SR-Latch ☐ SR-FF ☐ JK-FF ■ **1 bit counter.**

18. If multiple inputs of an encoder are set to 1 the output is :

    ☐ all bits are zero. ☐ all bits are one. ■ **Undefined.** ☐ The code of the first active line. ☐ The code of the last active one

19. The V output of an encoder is set to 1 if :

☐ All input lines are set to zero. ■ **All input lines are set to one.** ■ **the first line is set to one.** ■ **the last line is set to one.** ■ **at least one line is set to one.**

20. To build a 16x1 Mux using only 4x1 Mux we need :

☐ 4 4x1 Mux ■ **5 4x1 Mux** ☐ 6 4x1 Mux ☐ 7 4x1 Mux ☐ 8 4x1 Mux

21. The parity of two bits can be computed using :

☐ NOT gate. ☐ NOR gate. ☐ OR gate. ☐ XNOR gate. ■ **XOR gate.** ☐ AND gate. ☐ NAND gate.

22. In a D-latch Q change to 1 if :

☐ E =0 and D=0 ☐ E =0 and D=1 ☐ E =1 and D=0 ■ **E = 1 and D=1** ☐ Clock change and D=0. ☐ Clock change and D=1.

23. If we set the Clear input of a rising edge FlipFlop :

☐ Q is set to one immediately. ■ Q **is set to zero immediately.** ■ $\bar{Q}$ **is set to one immediately.** ☐ Q is set to zero on the next clock rise. ☐ Q is set to zero on the next clock fall. ☐ Q toggle on the next clock rise.

24. A clock signal is connected to an SR-Latch as follows ($R = CK$ and $R = C\bar{K}$ what do we get on the Q output of the latch ?

☐ Q is the same as the clock ■ Q **is the inverse of the clock.** ☐ Q is undefined ☐ Q is fixed at one. ☐ Q is fixed at zero.

25. To convert a D flipFlop to a SR flipflop

☐ Write S and R as a function of D ☐ Write D as a function of S and R ■ **Write D as a function of S,R and Q** ☐ Write S and R as a function of D and Q

26. To convert a D flipFlop to a SR flipflop

☐ We need Excitation table of SR and characteristic table of D ■ **We need Excitation table of D and characteristic table of SR**

27. left serial shift register can be used to :

☐ Perform serial addition. ■ **Perform serial communication.** ■ **Multiply by 2.** ☐ Divide by 2.

28. To connect a keyboard with 64 keys to a computer in parallel we use

☐ 6x64 decoder. ☐ 16x64 decoder. ■ **64x6 encoder.** ☐ 64x16 encoder. ☐ 64 bit PIPO register.

29. what type of registers we use to connect a keyboard to a machine :

☐ SISO →SISO ☐ SISO →SIPO ☐ PIPO →PIPO ■ **PISO →SIPO** ☐ PIPO →PIPO

30. To build an N bit serial adder we can use :

☐ 2 shift registers + 2 half adders. ■ **2 shift registers + 2 half adders + 1FF.**
☐ 1 shift register + N half adder. ☐ N shift register + 2 half adders + 1FF.

31. To build a modulo 4 asynchronous counter with T-FF (without PR/CR) we need

■ **2 T-FF** ☐ 2 T-FF and AND gate. ☐ 3 T-FF ☐ 3 T-FF and AND gate
☐ 4 T-FF ☐ 4 T-FF and AND gate

32. witch of the following sequences can be counted with an asynchronous counter :

☐ 0 1 3 4 0 1 3 4 0 …
■ **0 1 2 3 4 0 1 ...**
■ **0 1 2 3 4 1 2 3 4 1 2 ...**
■ **7 6 5 4 3 2 1 0 7 ...**
☐ 5 4 3 2 1 0 5 4 …

33. witch of the following sequences can be counted with a synchronous counter :

☐ 0 1 2 3 4 1 2 3 4 1 2 …
■ **0 1 2 3 4 0 1 ...**
■ **0 1 3 4 0 1 3 4 0 ...**
■ **7 6 5 4 3 2 1 0 7 ...**
■ **5 4 3 2 1 0 5 4 ...**

34. We need _____**8**_____ clock pulse(s) to read the value of a 8 bit PISO register.

35. We need _____**1**_____ clock pulse(s) to read the value of a 16 bit PIPO register.

36. We need _____**8**_____ clock pulse(s) to write the value of a 8 bit SISO register.

37. We need _____**16**_____ clock pulse(s) to write the value of a 16 bit SIPO register.

38. To display the value of a counter in Logisim we use **7 segmennt** display.

39. To make a module 5 asynchronous counter we connect _____Q_2_____ to an AND gate and we connect the output of the AND gate to **The CR inputs of all the FFs**

40. To connect a multi-bit input to the select lines of a multiplexer in Logisim we use __**Splitter**__