Machine structure 2

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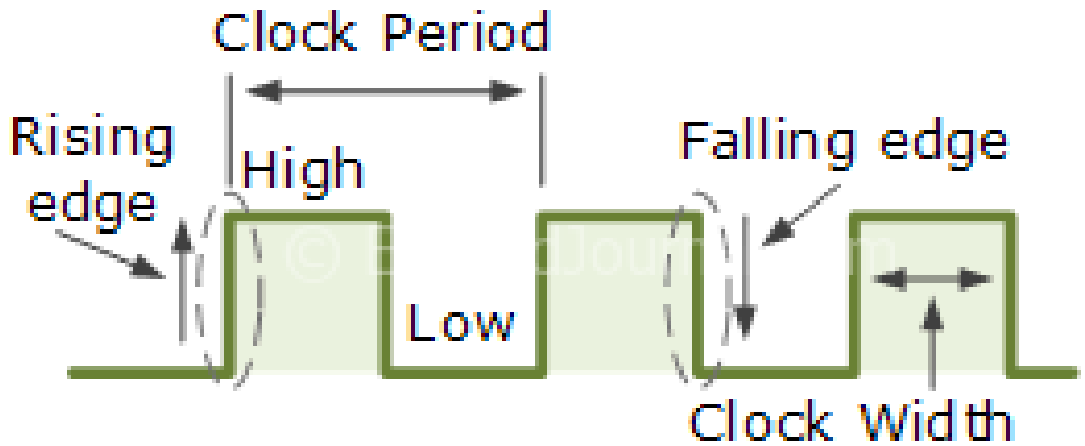
Sequential Circuits

The clock signal

- A clock pulse signal is a square wave. In a square wave, voltage varies by periodically switching from high to low state (no 'in between' values), it is therefore a digital signal as there are only two states.
- The period T of the clock pulse is the time in seconds taken for one complete cycle.
- The frequency f measured in hertz (Hz) of the clock cycle can be found by calculating the reciprocal of the period $f = \frac{1}{T}$.



Flip flops

- latches vs Flip flops
- Master slave D Flip-Flop
- Master-slave SR flip-flop
- JK-Flip flop
- JK timing diagram
- T-Flip Flop
- T Flip Flop timing diagram
- Asynchronous Set and Reset
- Interconversion of flip flops

Latch synchronization problem

- Provide us with a simple form of memory.
- Latch circuit responds any time the inputs change.
- We want to limit the state change to a very narrow time period witch will allow us to synchronize the state change of several devices.

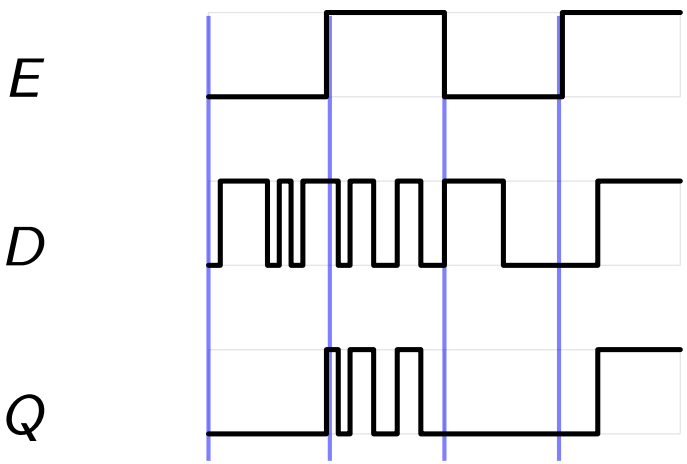
latches vs Flip flops

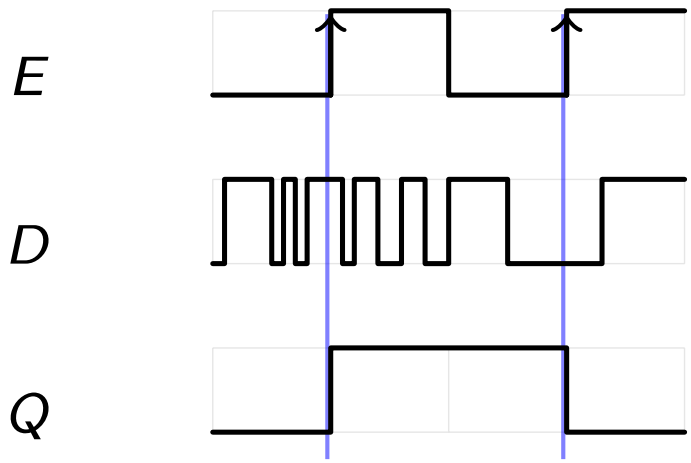
D latch

- As long as the clock signal is high any change in the value of input D appears in the output Q

D Flip flop

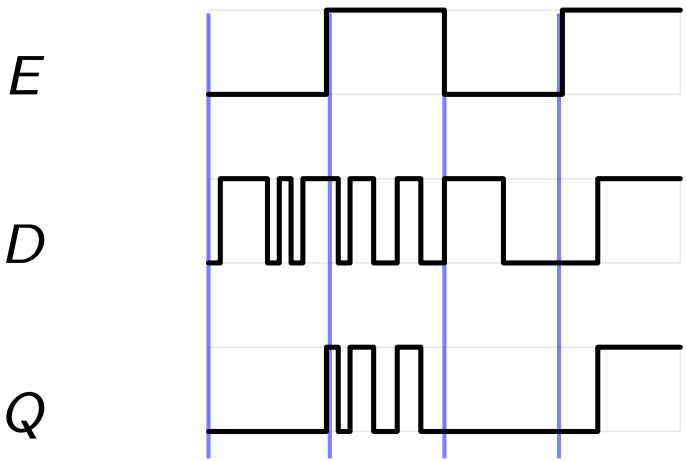
- Q changes only on the clock signal transition (rising edge) and the Flip flop is in latch state during all the clock cycle.

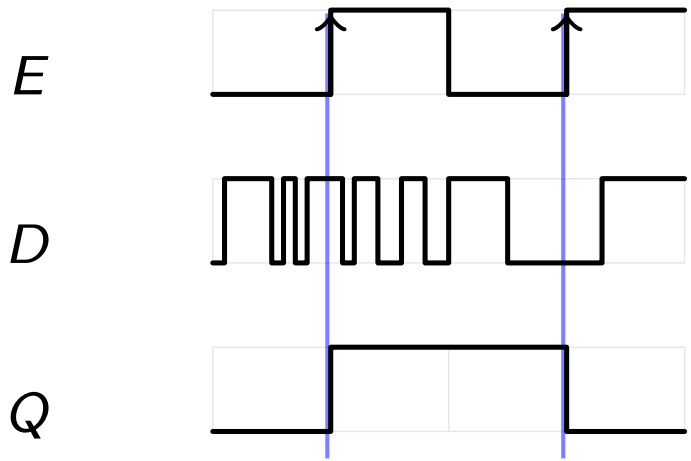




latches vs Flip flops

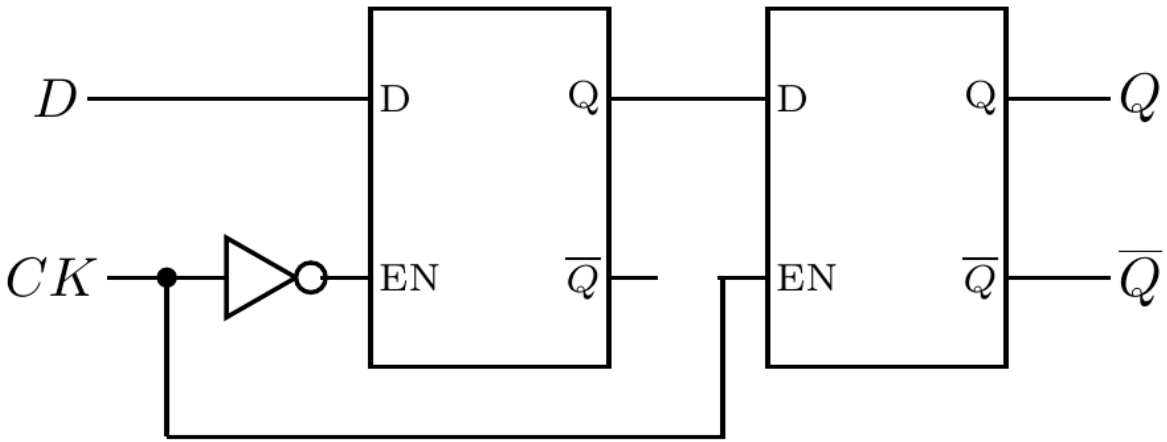
- A latch is sensitive to the level of the clock.
- A flip-flop is sensitive to the transition of the clock
- A latch is called a level-triggered memory element
- A flip-flop is called an edge-triggered memory element

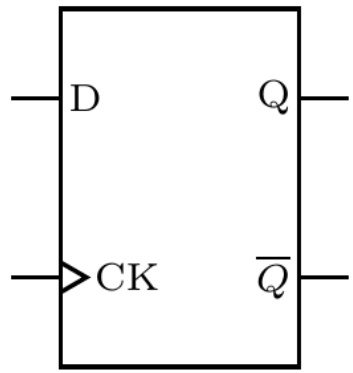




Master slave D Flip-Flop (positive edge ⎍)

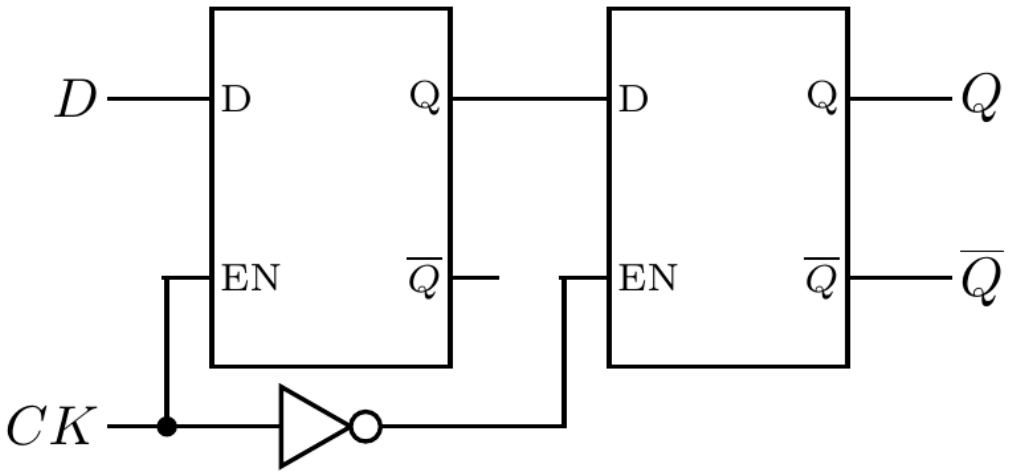
- A master-slave D flip-flop can be built from two D latches.
- The master latch is enabled when the clock is low and the slave is disabled.
- The slave latch is enabled when the clock is high and the master is disabled.
- When the clock transition from low to high the value stored in the master latch gets stored in the slave latch.
- The outputs change on the positive edge ⎍ of a pulse on the clock signal.

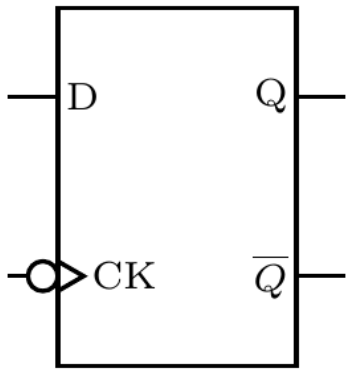




Master slave D Flip-Flop (negative edge ⎍)

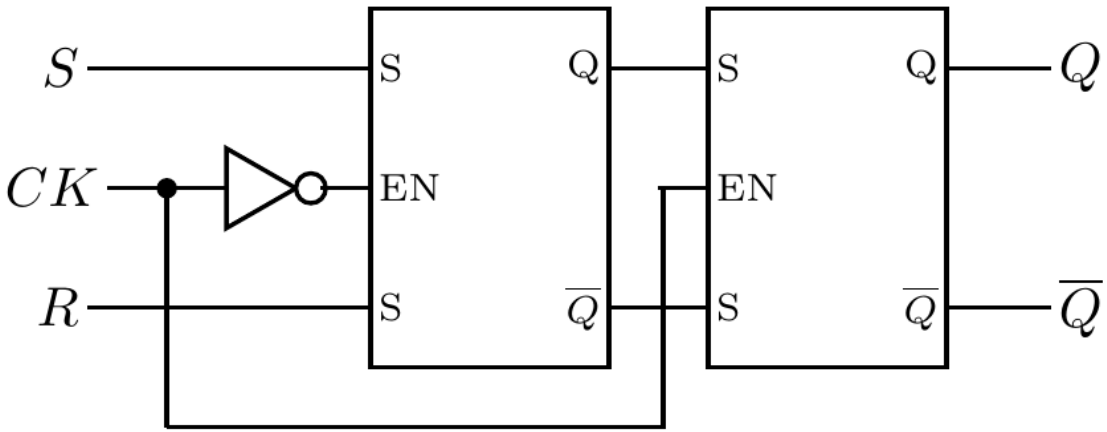
- The master latch is enabled when the clock is high and the slave is disabled.
- The slave latch is enabled when the clock is low and the master is enabled.
- When the clock transition from high to low the value stored in the master latch gets stored in the slave latch.
- The outputs change on the negative edge ⎍ of a pulse on the clock signal.

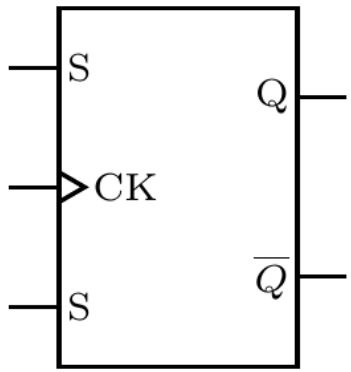




Master-slave SR flip-flop (positive edge ⎍)

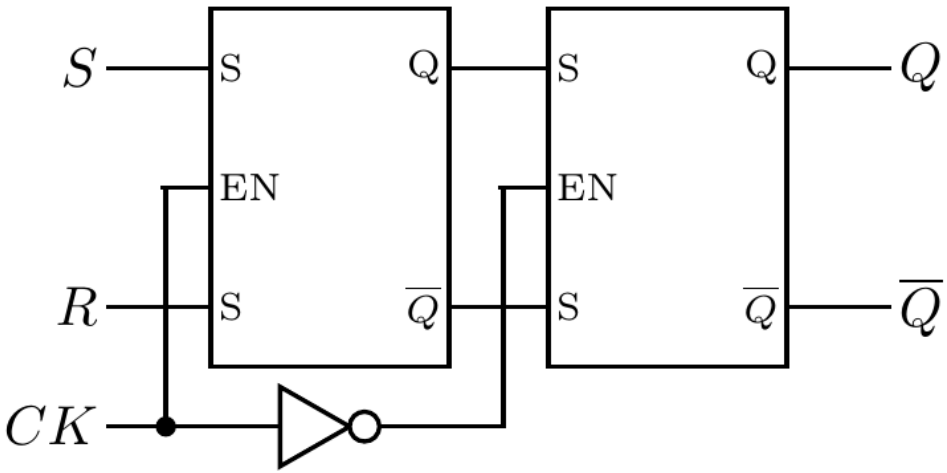
- A master-slave SR flip-flop can be built from two SR latches.
- The master latch is enabled when the clock is low and the slave is disabled.
- The slave latch is enabled when the clock is high and the master is disabled.
- When the clock transition from low to high the value stored in the master SR latch gets stored in the slave SR latch.
- The outputs change on the positive edge ⎍ of a pulse on the clock signal.

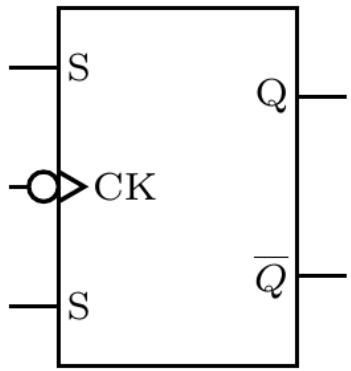




Master slave SR Flip-Flop (negative edge ⎍)

- The master latch is enabled when the clock is high and the slave is disabled.
- The slave latch is enabled when the clock is low and the master is enabled.
- When the clock transition from high to low the value stored in the master SR latch gets stored in the slave SR latch.
- The outputs change on the negative edge ⎍ of a pulse on the clock signal.

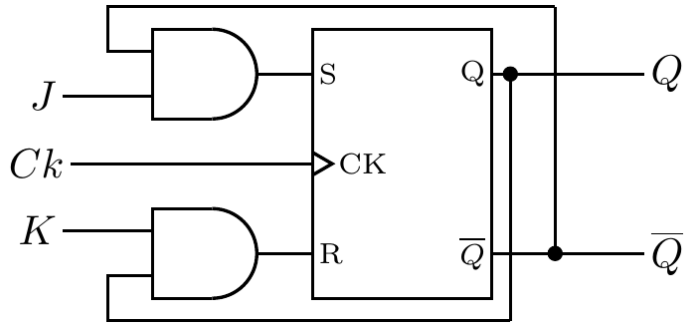




JK-Flip flop

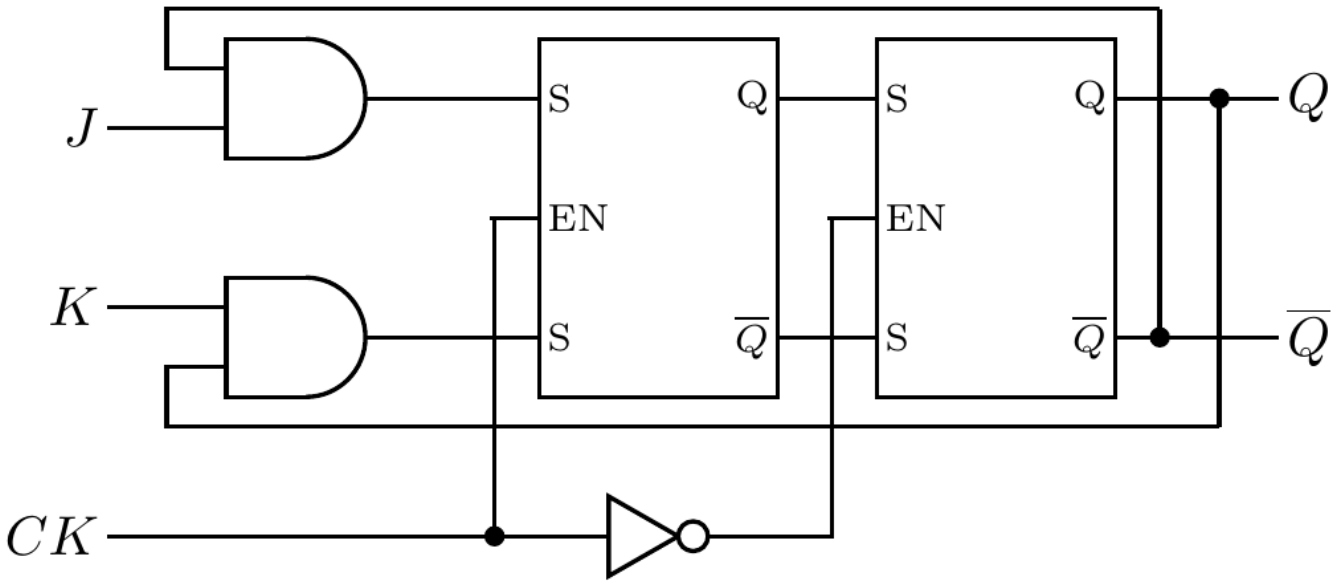
The JK-flip flop represents an enhancement over the SR flip flop by addressing the issue of the forbidden state through the incorporation of feedback. The JK-Flip flop, originally named after its inventor, Jack Kilby

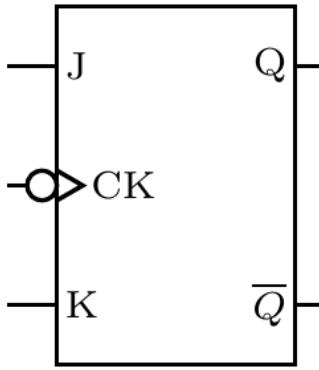
E	J	K	Q	$\bar{Q}$	operation
0	x	x	latch	latch	memory
1	0	0	latch	latch	memory
1	0	1	0	1	reset
1	1	0	1	0	set
1	1	1	toggle	toggle	invert



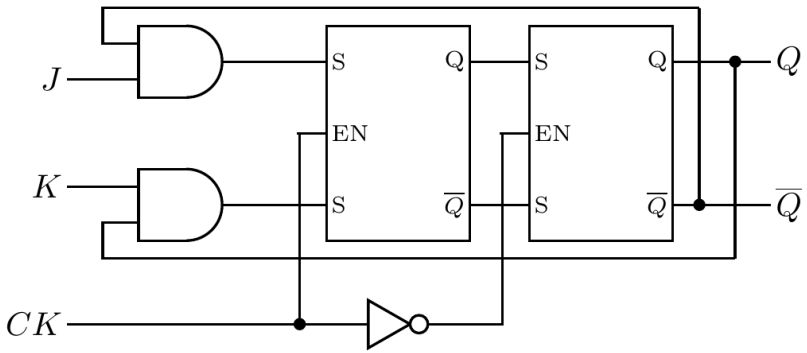
Master slave JK Flip-Flop (negative edge ⎍)

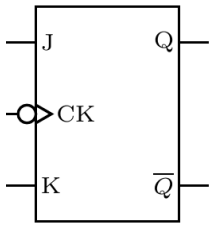
- The master latch is enabled when the clock is high and the slave is disabled.
- The slave latch is enabled when the clock is low and the master is enabled.
- When the clock transition from high to low the value stored in the master SR latch gets stored in the slave SR latch.
- The outputs change on the negative edge ⎍ of a pulse on the clock signal.





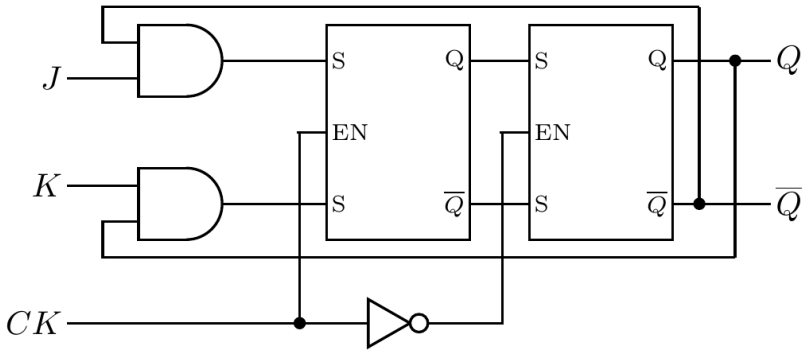
JK Flip-Flop (Characteristic table)

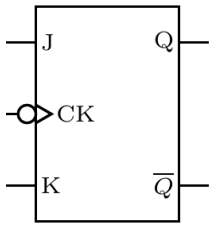




J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

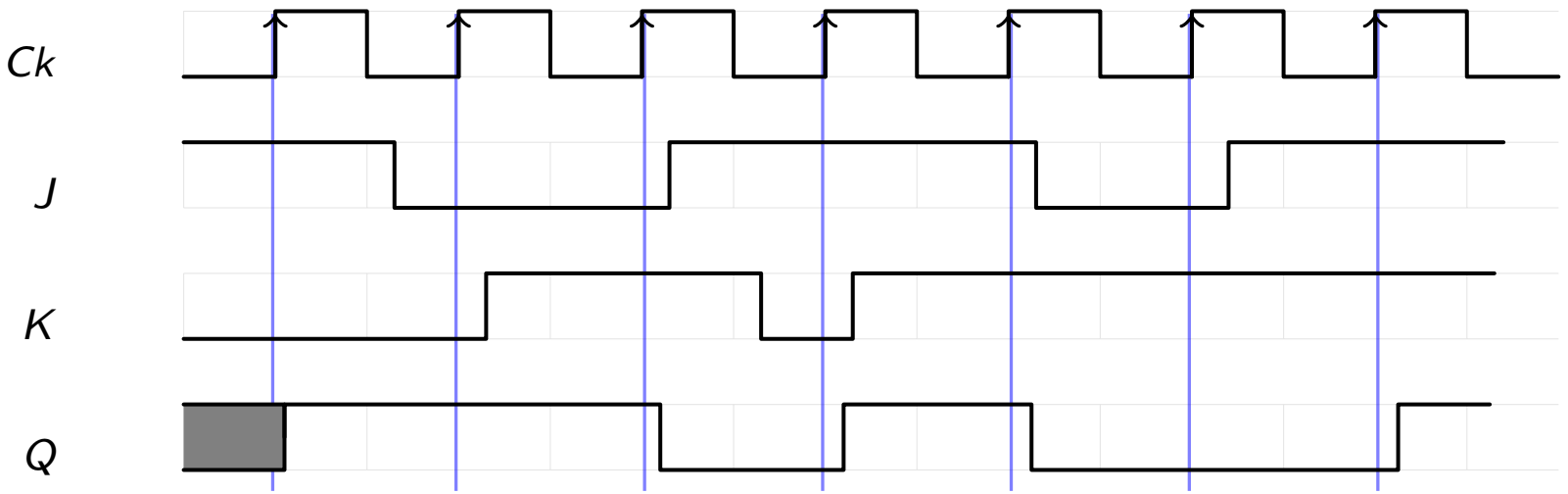
JK Flip-Flop (Excitation table)





Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

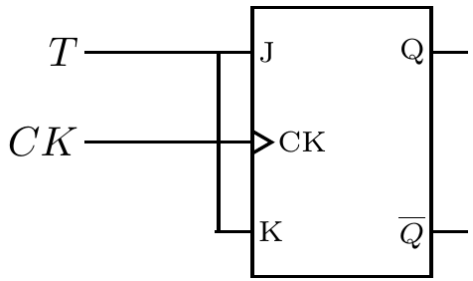
JK timing diagram (positive edge ⎍)



T-Flip Flop

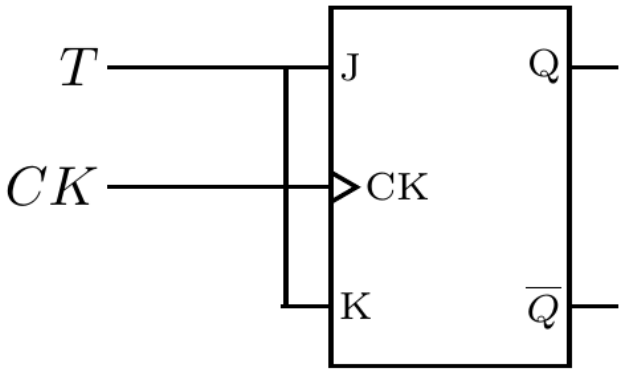
The T-flip flop is essentially a modification of the JK flip flop, where the J and K inputs are tied together and connected to the toggle input T. When the toggle input is activated, the output of the T latch changes state, toggling between its two possible states (0 and 1).

E	T	Q	$\bar{Q}$	operation
0	x	latch	latch	memory
1	0	latch	latch	memory
1	1	toggle	toggle	invert

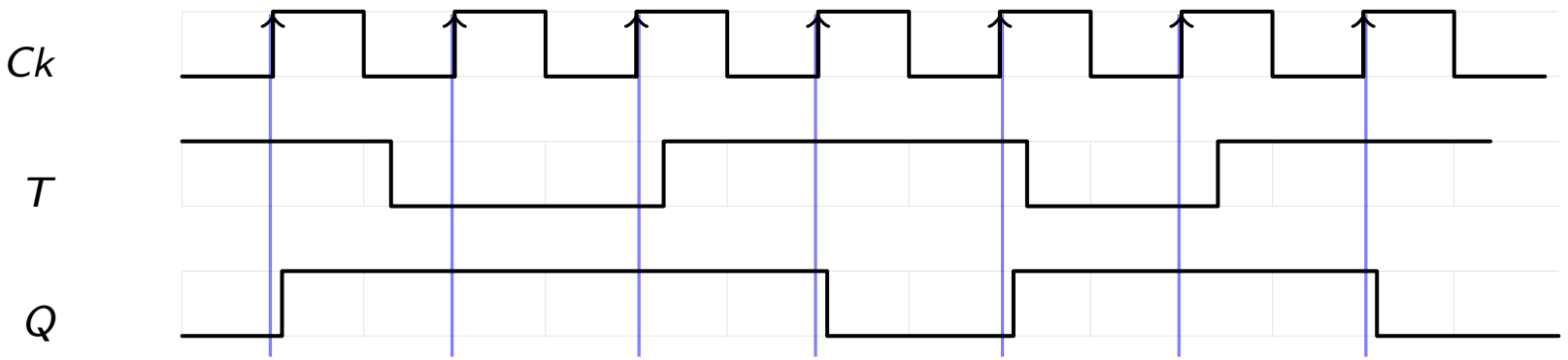


T Flip-Flop

- T flip flop is known as Toggle Flip Flop because it can toggle (flip) its output depending on the input T.
- T here stands for Toggle.
- Toggle basically indicates that the output Q will be flipped either from 1 to 0 or from 0 to 1.
- if T is zero the flip flop will remain on memory state (latch state)
- if T is one during a clock transition the value of Q will flip.

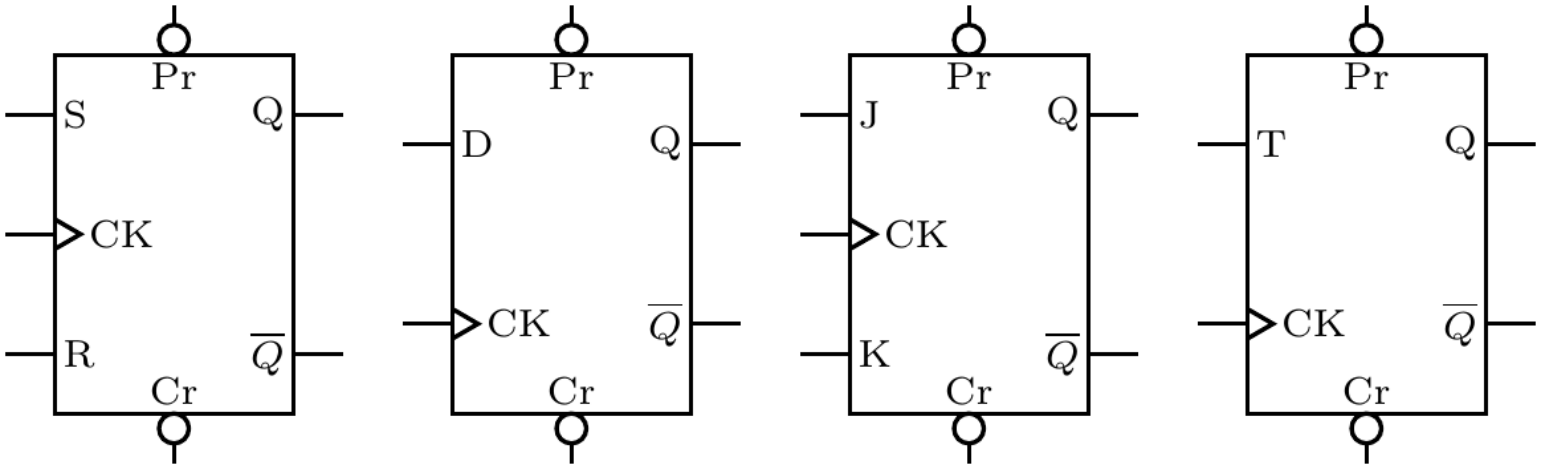


T Flip Flop timing diagram (positive edge ⎍)

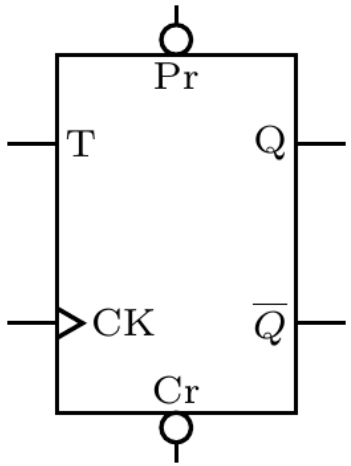


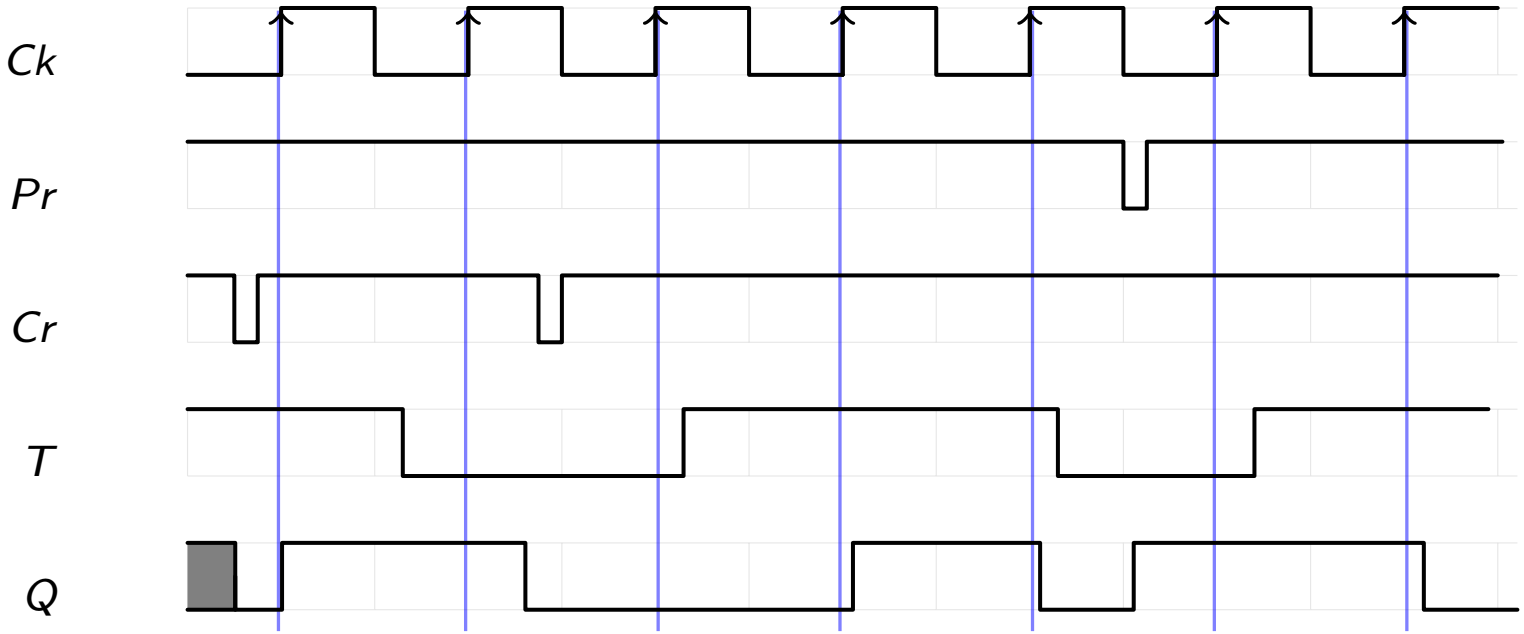
Asynchronous Set and Reset

- When Flip-Flops are powered, their initial state is unknown
- We can add asynchronous Preset and Clear inputs taht work independently of the clock.
- Prset forces Q to become immediately 1, independently of the clock.
- Clear forces Q to become immediately 0, independently of the clock.



Asynchronous Set and Reset





Interconversion of flip flops

To convert a flip flop of type X to a flip flop of type Y we follow these steps:

- fill the characteristic table of the target flip flop Y
- fill the excitation table of the source flip flop X
- Get the simplified expressions for each excitation input (X inputs) as a function of Y inputs and the current state (use kmap if needed).
- Draw the circuit diagram of desired flip-flop according to the simplified expressions using given flip-flop and necessary logic gates

Conversion of an S-R Flip-flop to a D Flip-flop

To convert SR flip flop to a D flip flop follow these steps:

- fill the characteristic table of the D flip flop.
- fill the excitation table of the SR flip flop.
- Get the simplified expressions for each excitation input (SR inputs) as a function of D inputs and the current state (use kmap if needed).
- Draw the circuit diagram of desired flip-flop according to the simplified expressions using given flip-flop and necessary logic gates

Conversion of an S-R Flip-flop to a D Flip-flop

1 D characteristic table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

2 SR excitation table

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

SR to D conversion table

D	Q_n	S	R
0	0	0	x
0	1	0	1
1	0	1	0
1	1	x	0

$R = \overline{D}$

$S = D$

Conversion of D Flip-flop to an SR Flip-flop

Table: SR characteristic table

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

Table: D excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

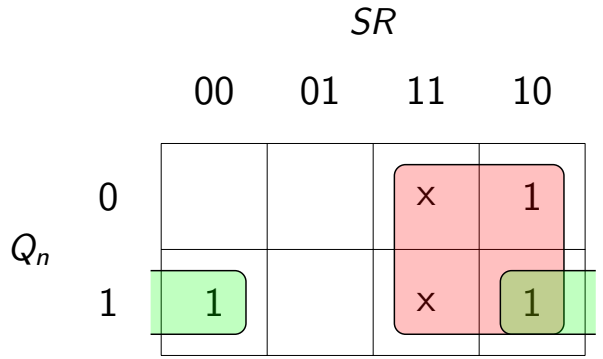
Table: D to SR conversion table

S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	x	x
1	1	1	x	x

Conversion of D Flip-flop to an SR Flip-flop

Table: D to SR conversion table

S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	x	x
1	1	1	x	x



$$D = S + \bar{R}Q_n$$