Machine structure 2

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Sequential Circuits

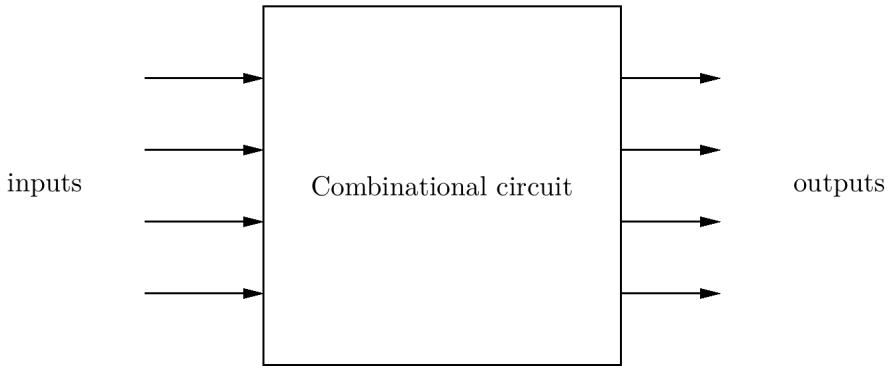
Introduction

Logic circuits for digital system may be Combinational or sequential

- Combinational circuit
  - consists of logic gates whose outputs at any time are determined directly from the present combination of inputs without regard to previous inputs.
  - Outputs are a function of (only) the inputs inputs .
- Sequential circuit
  - Outputs are a function of the inputs and the previous state of the outputs.
  - Add memory elements in addition to logic gates.
  - As a consequence, the output depend not only on present input, but also on past inputs and the circuit behavior must be specified by a time sequence of inputs and internal states.

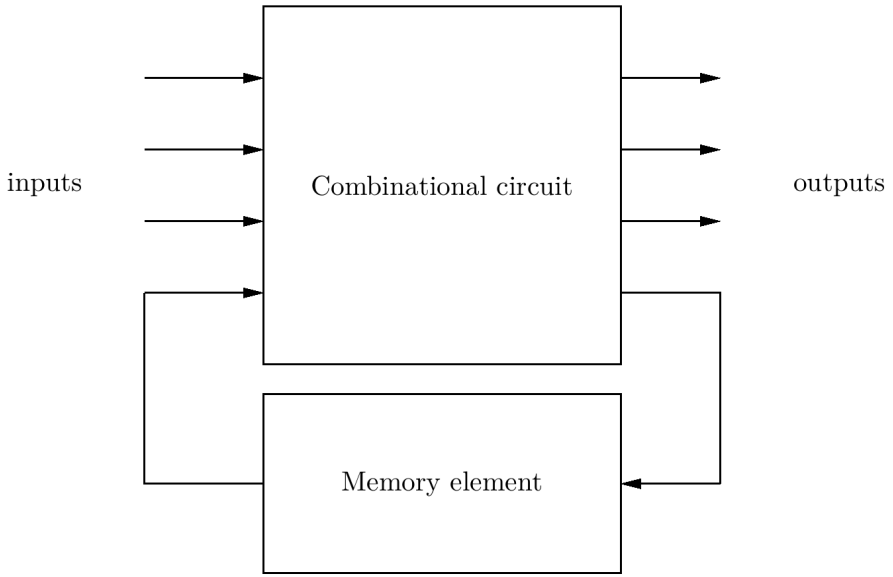
Combinational circuits

- Combinational circuit :
  - Consists of logic gates whose outputs at any time are determined directly from the present combination of inputs without regard to previous inputs.
  - Outputs are a function of (only) the inputs inputs .



Sequential Circuits

- The logic circuits discussed previously are known as combinational, in that the output depends only on the condition of the latest inputs
- However, we will now introduce a type of logic where the output depends not only on the latest inputs, but also on the condition of earlier inputs. These circuits are known as sequential, and implicitly they contain memory elements

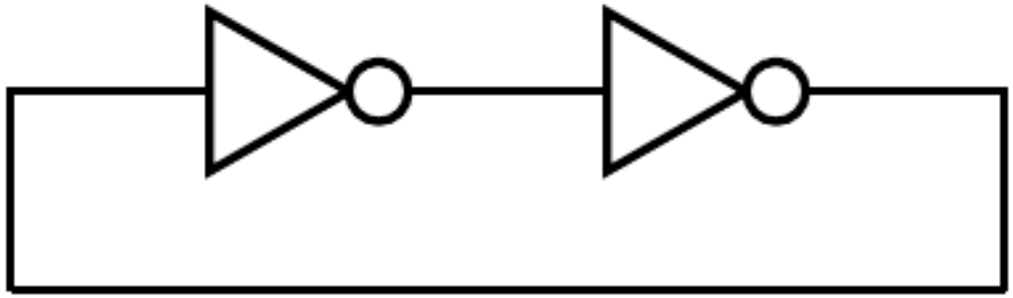


Latches

- NOT Gate bistable latch
- SR latch
- Gated SR-Latch
- D-Latch (Data latch)
- Characteristic & excitation table.
- Timing diagram
- The clock signal
- latches vs Flip flops

NOT Gate bistable latch

At the heart of a bistable circuit are two inverting logic gates. The output of each logic gate is connected to the input of the other gate. Such a circuit has two states where it is stable.



NOT Gate bistable latch

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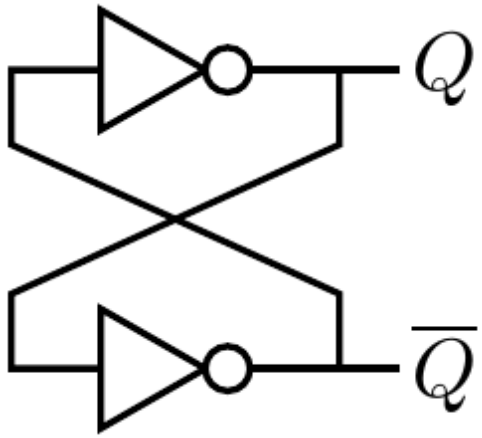
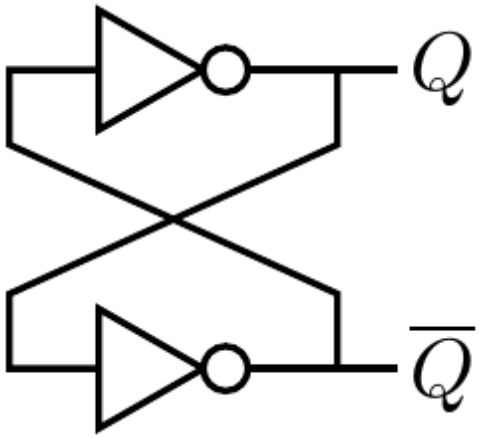


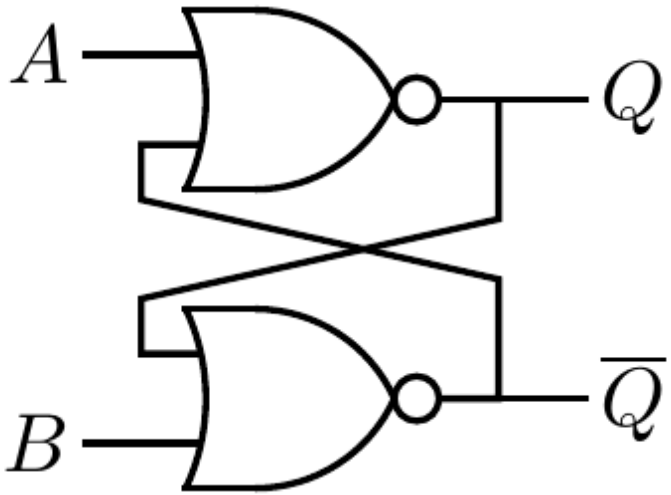
NOT Gate bistable latch

The problem of the NOT gate bistable is that we have no way to change the state of the latch !.



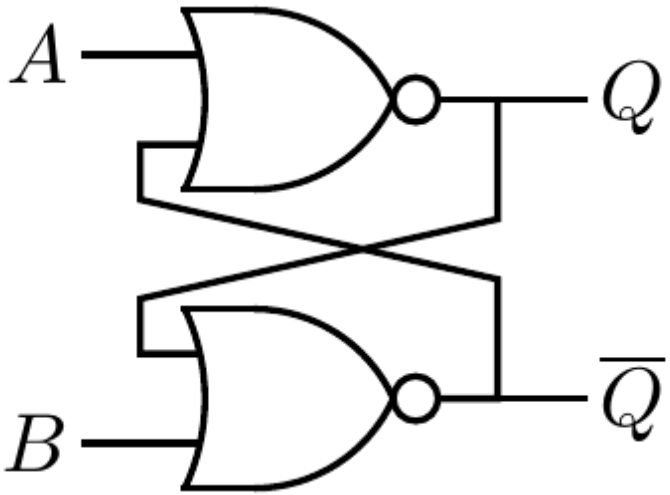
NOR Gate bistable latch

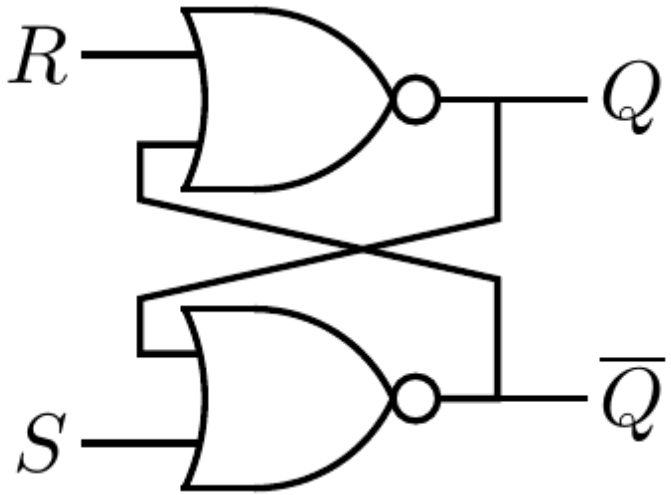
- Consider the following circuit:
  - When $A = 1$ and $B = 0$: Q will be 1 and $\bar{Q}$ will be 0
    - Therefore A is acting like a RESET signal when set to 1.
  - When $B = 1$ and $A = 0$: Q will be 1 and $\bar{Q}$ will be 0
    - Therefore B is acting like a SET signal when set to 1.
  - When $A = 0$ and $B = 0$ then the two NOR gates acts like NOT gates !
    - Therefore the circuit acts like a bistable latch circuit and keeps the last state.
  - When $A = 1$ and $B = 1$: Q and $\bar{Q}$ both are 0 and the circuit is in the forbidden state



NOR Gate SR latch (SET/RESET)

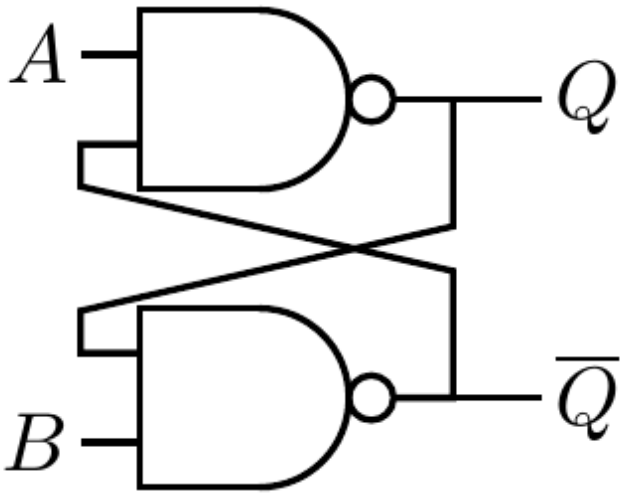
- Consider the following circuit:
  - When $A = 1$: $Q = 0$ therefore A is acting like a RESET signal and can be renamed R.
  - When $B = 1$: $Q = 1$ therefore B is acting like a SET signal and can be renamed S.
  - The circuit is called NOR Gate SR Latch





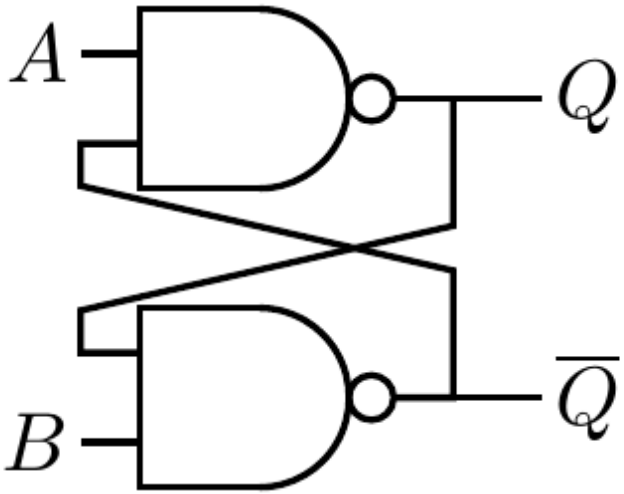
NAND Gate SR latch

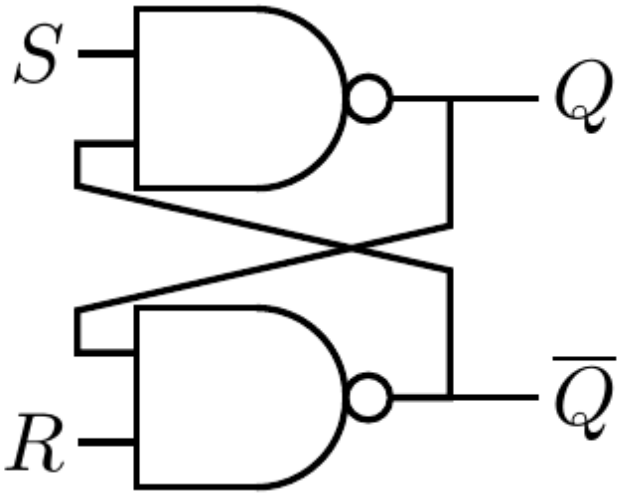
- Consider the following circuit:
  - When $A = 0$ and $B = 1$: Q will be 1 therefore A is acting like a SET signal when set to 0.
  - When $B = 0$ and $A = 1$: Q will be 0 therefore B is acting like a RESET signal when set to 0.
  - When $A = 1$ and $B = 1$ then the two NAND gates acts like NOT gates and the circuit acts like a NOT gate bistable LATCH !.
  - When $A = 0$ and $B = 0$: Q and $\bar{Q}$ both are 1 and the circuit is in the forbidden state!



NAND Gate SR latch (SET/RESET)

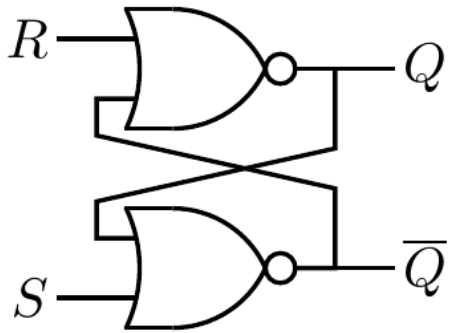
- Consider the following circuit:
  - When $A = 0$: $Q = 1$ therefore A is acting like a SET signal and can be renamed S.
  - When $B = 0$: $Q = 0$ therefore B is acting like a RESET signal and can be renamed R.
  - The circuit is called NAND Gate SR Latch
  - Since the circuit reacts when S or R are set to zero, we call it an active low circuit.





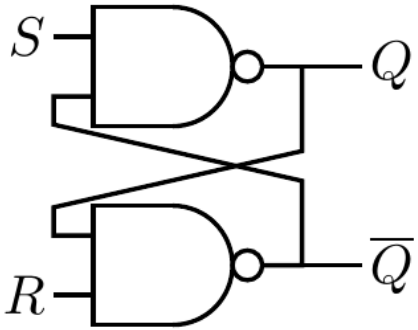
SR latch

NOR SR Latch active high



S	R	Q	$\bar{Q}$	operation
0	0	latch	latch	memory
0	$\underline{1}$	0	1	reset
$\underline{1}$	0	1	0	set
1	1	?	?	forbidden

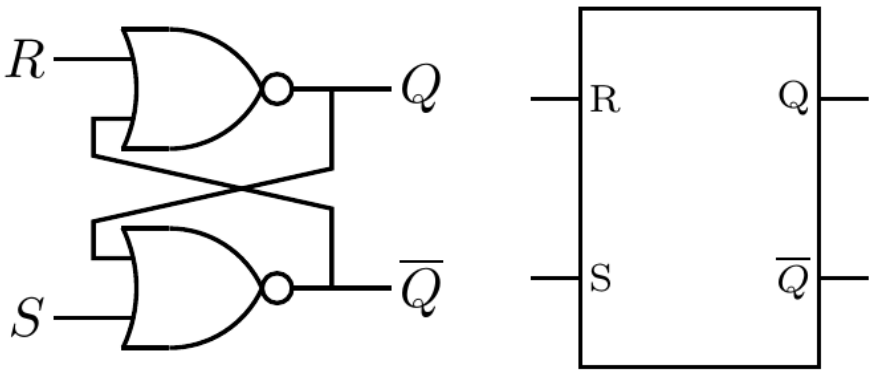
NAND SR Latch active low



S	R	Q	$\bar{Q}$	operation
0	0	?	?	forbidden
$\underline{0}$	1	1	0	set
1	$\underline{0}$	0	1	reset
1	1	latch	latch	memory

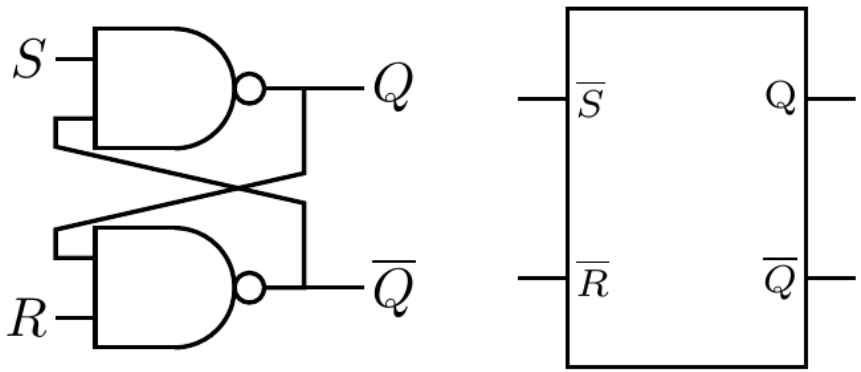
SR latch

NOR SR Latch active high



S	R	Q	$\bar{Q}$	operation
0	0	latch	latch	memory
0	1	0	1	reset
1	0	1	0	set
1	1	?	?	forbidden

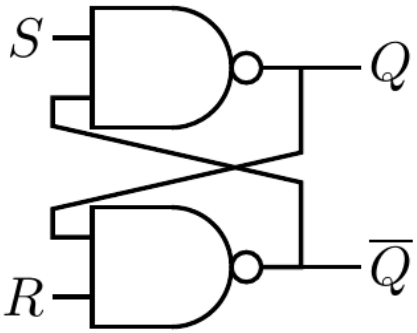
NAND SR Latch active low

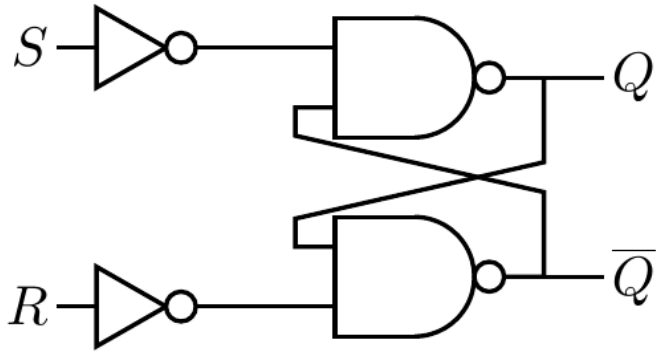


S	R	Q	$\bar{Q}$	operation
0	0	?	?	forbidden
0	1	1	0	set
1	0	0	1	reset
1	1	latch	latch	memory

SR latch

We can convert an active lox latch to an active low high and vise versa.





S	R	Q	$\bar{Q}$	operation
0	0	?	?	forbidden
0	1	1	0	set
1	0	0	1	reset
1	1	latch	latch	memory

NAND SR Latch active low

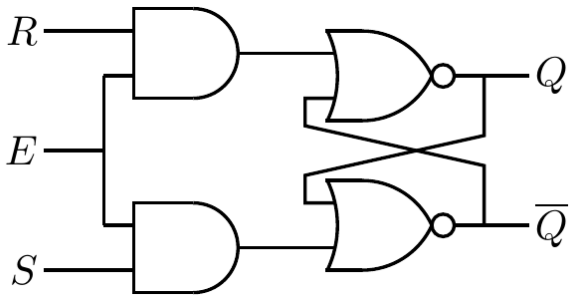
S	R	Q	$\bar{Q}$	operation
0	0	latch	latch	memory
0	1	0	1	reset
1	0	1	0	set
1	1	?	?	forbidden

NAND SR Latch active high

Gated SR-Latch

- A Gated SR-Latch is an update of the SR-Latch where :
  - An additional (enable) input signal E is added.
  - Enable controls when the state of the latch can be changed.
  - When $E = 0$, the S and R inputs have no effect on the latch. The latch remains in the same state regardless of S and R
  - When $E = 1$, the circuit behaves as a normal SR latch.

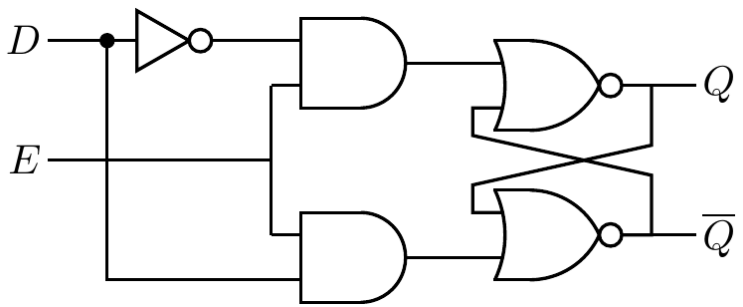
E	S	R	Q	$\bar{Q}$	operation
0	x	x	latch	latch	memory
1	0	0	latch	latch	memory
1	0	1	0	1	reset
1	1	0	1	0	set
1	1	1	?	?	forbidden



D-Latch (Data latch)

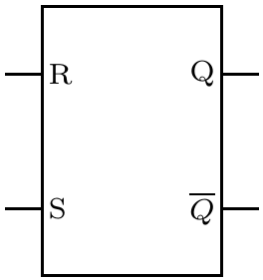
D-latches, also referred to as transparent latches, are constructed using gated SR-latches.the D input is connected to the S input, and an inverter is inserted between the D input and the R input. This arrangement ensures that both the S and R inputs cannot be simultaneously set to 1, thus eliminating the problematic scenario encountered in a basic SR-latch.

E	D	Q	$\bar{Q}$	operation
0	x	latch	latch	memory
1	0	0	1	reset
1	1	1	0	set



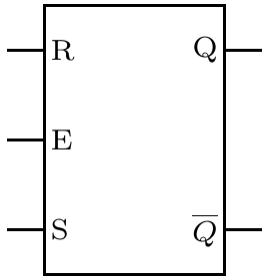
SR and D Latch summery

SR-Latch



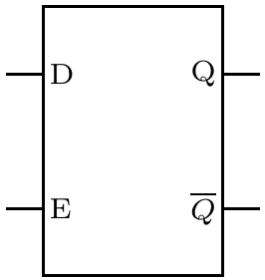
S	R	Q	$\bar{Q}$	operation
0	0	latch	latch	memory
0	1	0	1	reset
1	0	1	0	set
1	1	?	?	forbidden

Gated SR-Latch



E	S	R	Q	$\bar{Q}$	operation
0	x	x	latch	latch	memory
1	0	0	latch	latch	memory
1	0	1	0	1	reset
1	1	0	1	0	set
1	1	1	?	?	forbidden

D-Latch



E	D	Q	$\bar{Q}$	operation
0	x	latch	latch	memory
1	0	0	1	reset
1	1	1	0	set

Characteristic table of SR-Latch

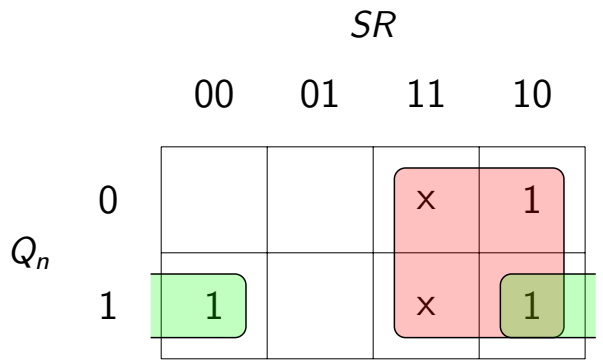
- The characteristic table gives us an idea about the behavior of a given latch. We know that the next state of a latch output Q_{n+1} depends on the present inputs as well as the present output Q_n. So in order to know the next state output of a latch, we have to consider the present state output also.

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x

Characteristic table of SR-Latch

- The characteristic table of an SR-Latch is given in the table below. From the characteristic table we have to find out the characteristic equation of the SR-latch.

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	x
1	1	1	x



$$Q_{n+1} = S + \bar{R}Q_n$$

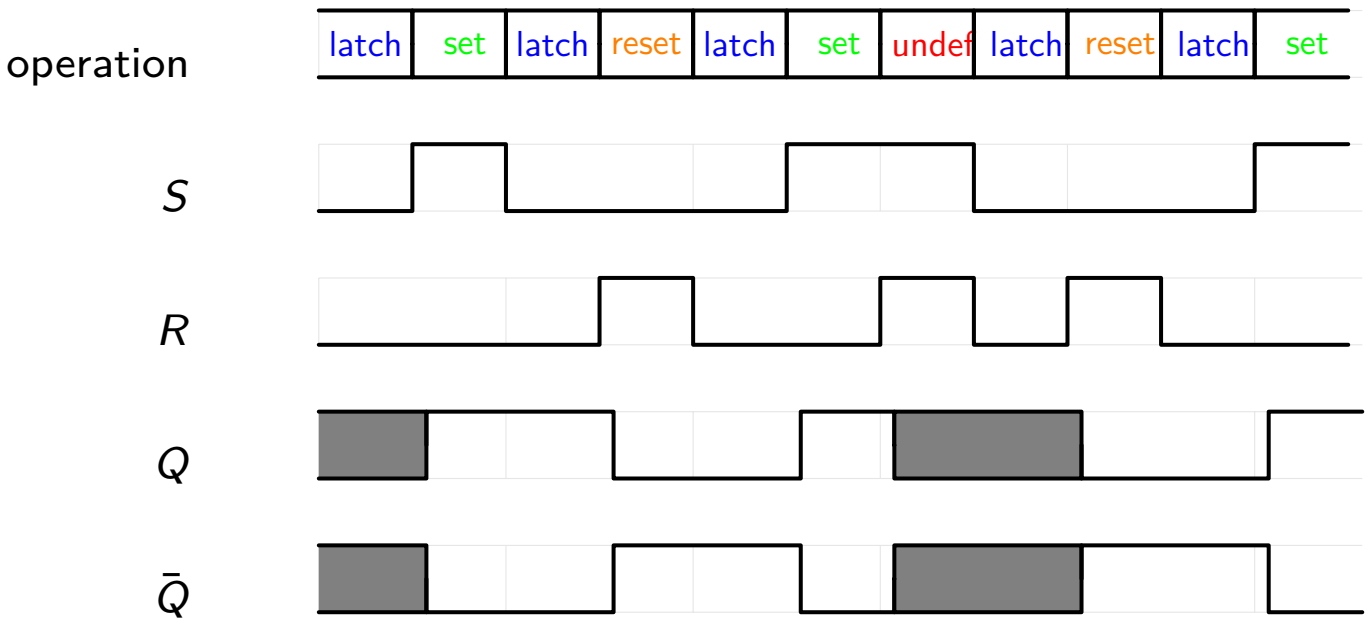
The excitation table of SR-Latch

- An excitation table defines the latch input variables as a function of the current state Q_n and the next state Q_{n+1}.

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

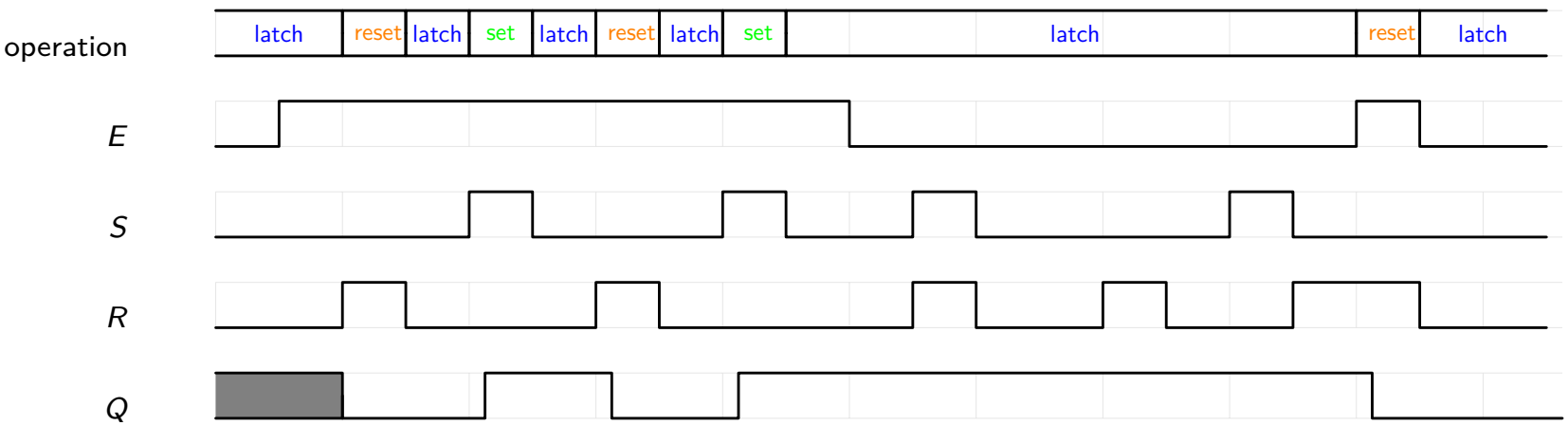
SR-Latch Timing diagram

- The operation of any latch can be described using a timing diagram.
- Q is undefined until set or reset is used



Gated SR-Latch Timing diagram

- Q is undefined until set or reset is used
- When E is 0 S and R has no effect on the latch.



D-Latch timing diagram

- Q is undefined until E is high (set to 1).
- When E is 0 D has no effect on the latch (memory).
- When E is 1 Q takes the same value of D.