Ministry of Higher Education and Scientific Research

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Fundamental Electronics
Problems & Exercises (of Chap 3)
Bipolar Transistors
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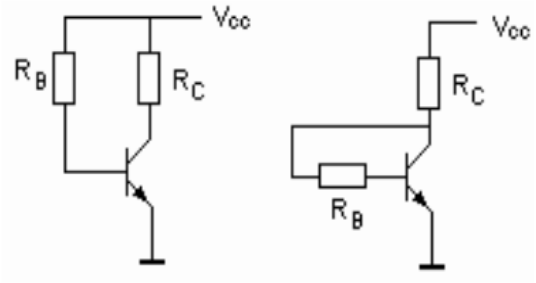
Exercise 1

Calculate the resistor values required to bias a silicon **NPN** transistor in each of the two circuits shown below.



Given: **β = 100, V_{CC} = 10 V**

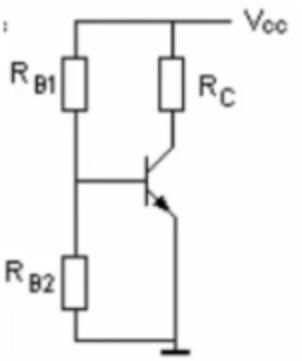
It is desired that the quiescent operating point be fixed at:

V_{CE0} = 5 V, I_{C0} = 1 mA.

with: **V_{BE0} = 0.7 V**

Exercise 2

An **NPN** silicon transistor is biased using a base voltage divider, as shown in the circuit diagram.



Given: **β = 100** and **V_{CC} = 10 V**

The desired operating point (bias point) is defined by:

V_{CE0} = 5 V, I_{C0} = 1 mA, V_{BE0} = 0.7 V

1. Determine the Thevenin equivalent model between the base of the transistor and ground.
2. Deduce the equation of the input load line (base circuit load line).
3. Assuming that **RB1** is 100 times greater than **RB2**, calculate the values of the resistors **RB1**and **RB2**.
4. Derive the equation of the output load line.
5. Calculate the value of the collector resistor **R_C**

Exercise 3