Exercise Series N°04 : Memory Management

Exercise V.1: (Understanding Questions)

Q1) Name two differences between logical and physical addresses.

Q2) Explain the difference between internal and external fragmentation.

Q3) Which component of the CPU is used to implement virtual memory?

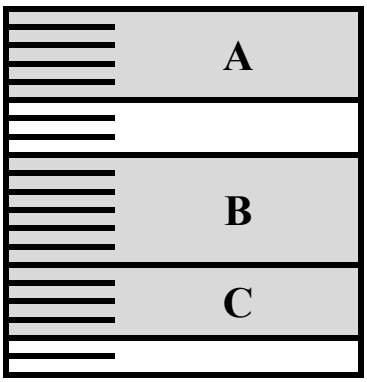
Q4) What is swapping?

Q5) What is virtual memory?

Q6) Why are page sizes always powers of 2?

Q7) Explain, why virtual memory helps to better utilize the main memory.

Exercise V.2: (Bitmap & Linked List)



The following diagram shows the occupation of the Main Memory in allocation units (blocks) by processes A, B and C.

Q1) Give the schematics of the corresponding Bitmap and Linked List.

Q2) In the case where process B finishes its execution, update the Bitmap and Linked List for this new situation.

Exercise V.3: (Contiguous Memory Management Memory)

Q1) How is memory divided in the single contiguous memory management approach?

Q2) When a program is compiled, where is it assumed that the program will be loaded into memory? That is, where are logical addresses assumed to begin?

Q3) In a single contiguous memory management approach, if the logical address of a variable is **L** and the beginning of the application program is **A**, what is the formula for binding the logical address to the physical address?

Q4) If, in a single contiguous memory management system, the program is loaded at address **30215**, compute the physical addresses (in decimal) that correspond to the following logical addresses:

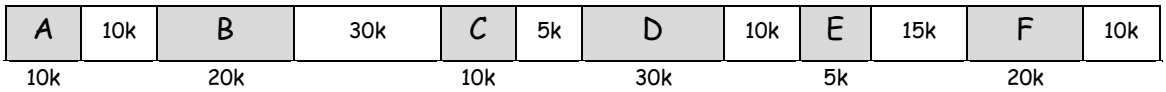
- **A.** 9223
- **B.** 2302
- **C.** 7044

Q5) If, in a **fixed partition** memory management system, the current value of the **base register is 42993** and the current value of the **limit register is 2031**, compute the physical addresses that correspond to the following logical addresses:

- **A.** 104
- **B.** 1755
- **C.** 3041

Exercise V.4: (First-fit, Best-fit, Worst-fit)

Given memory partition below



The shaded areas are allocated blocks, the white areas are free blocks

Using the following placement algorithms First Fit, Best Fit and Worst Fit, represent the evolution of the memory as a function of the arrival of the following successive events :

1) Arrival of program **G (20k)**
2) Program **B** leaves
3) Arrival of program **H (15k)**
4) Program **E** leaves
5) Arrival of program **I (40k)**

Exercise V.5: (Buddy System)

Simulate the management of an initially empty memory of size 1MB, using binary Buddy system allocation for the following allocation (+) and release (-) requests:

+70K, +35K, +80K, -70K, +60K, -35K, -60K, -80K

Exercise V.6: (Virtual Addresses)

Consider a logical address space of **64 pages** of **1024 words** each, mapped onto a physical memory of **32 frames**.

Q1) How many bits are there in the logical address and the physical address?

Let's assume that a computer's physical memory is divided into **4 frames** (from **0** to **3**) of **256 bytes**. In other words, physical memory is **1 KB** (**256 × 4 = 1 KB**).

Let's assume that a process has **3 KB** of virtual space (i.e. **12 pages**, from **0** to **11**) and successively refers to the following virtual addresses:

249, 255, 300, 500, 540, 600, 650, 700, 750, 800, 900, 1200.

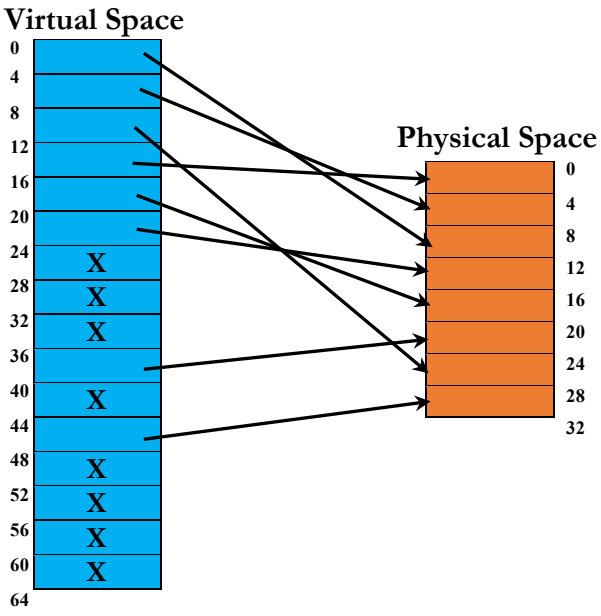
Q2) For each virtual address, find the virtual page number and offset?

Exercise V.7: (Address Translation)

The following diagram shows the mapping between virtual and physical addresses in a virtual (logical) memory system (**4KB page**). Physical memory corresponds to **8 pages**.

Complete the following table:

Virtual address	Physical address
20	....
4100	....
....	24684
26000	....



Exercise V.8: (Paging & Convert Logical Addresses to Physical Addresses)

Consider a system using paging technology and having the following characteristics:

- A page table of size **128 KB**
- Each page table entry contains a reference to a frame and a presence/absence bit.
- The size of a page is **64 KB**
- The size of physical memory is **2 GB**
- A virtual address is indexed by **1 Byte**

Answer the following questions, always justifying your answer:

Q1) How many frames does physical memory contain?

Q2) What is the size of a page table entry in bits?

Q3) How many entries are there in the page table?

Q4) What is the virtual memory size of this architecture?

Q5) What is the size of the address bus in bits for this system?

Q6) Consider the following two logical addresses expressed in decimal: **1024** and **65540**.

If possible, give the corresponding physical addresses (in decimal) based on the first **10** entries in the page table given below.

Page Number	Frame Number	Presence/Absence Bit
0	0	1
1	2	0
2	8	0
3	2050	1
4	21054	1
5	31463	1
6	2187	0
7	260	0
8	1266	0
9	1024	1

Exercise V.9: (Paging & Convert Physical Addresses to Logical Addresses)

Consider a system using paging technology and having the following characteristics:

- A page table with **2^{16} entries**
- Each page table entry is coded on **16 bits**. An entry contains a page frame number and a presence/absence bit.
- The offset (displacement) is coded on **16 bits**
- A virtual address is indexed by **1 Byte**

Answer the following questions, always justifying your answer:

Q1) What is the size of a page?

Q2) What is the size of physical memory?

Q3) What is the size of virtual memory?

Q4) What is the size of the address bus in bits for this system?

Q5) Considering the first eight entries of the page table represented by the following table, give the logical addresses corresponding to the physical addresses **33792** and **66048**.

Frame Number	Page Number	Presence/Absence Bit
7	0	0
6	0	0
5	0	1
4	1	1
3	0	0
2	0	0
1	2	1
0	3	1

Exercise V.10: (Page Replacement Algorithms)

A process has four-page frames allocated to it. (All the following numbers are decimal, and everything is numbered starting from zero). The time of the last loading of a page into each page frame, the time of last access to the page in each page frame, the virtual page number in each page frame, and the referenced (R) and modified (M) bits for each page frame are as shown (the times are in clock ticks from the process start at time zero to the event -- not the number of ticks since the event to the present).

Virtual Page Number	Frame	Time Loaded	Time Referenced	R (bit)	M (bit)
2	0	60	164	1	1
1	1	30	166	1	0
0	2	150	162	0	1
3	3	20	163	1	1

A page fault to virtual page 4 has occurred. Which page frame will have its contents replaced for each of the following memory management policies: **FIFO**, **LRU**, and **Second-Chance**.

Explain why in each case.

Exercise V.11: (Page Faults)

Consider the following page reference string: **0, 1, 4, 2, 0, 1, 3, 0, 1, 4, 2, 3.**

Q1) Assuming demand paging with **three frames**, how many page faults would occur for the following replacement algorithms : **FIFO, LRU** and **Optimal**.

Q2) Assuming demand paging with **four frames**, how many page faults would occur for the following replacement algorithms : **FIFO,** and **LRU**.

Exercise V.12: (Page Faults)

A program has a virtual space of **600 words**. Consider the sequence of virtual addresses:

34, 123, 145, 510, 456, 345, 412, 10, 14, 12, 234, 336, 412.

Q1) Give the sequence of referenced page numbers, knowing that they comprise **100 words**.

Q2) The program has **300 words** in main memory. Calculate the page fault rate (assuming initially empty memory) for the **OPT** (Optimal), **FIFO** (First Page In, First Page Out), **LRU** (Least Recently Used), and **Second-Chance FIFO** algorithms.